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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,498	YELURI, SHARADA	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,21-24,26,28 and 30* is/are pending in the application.

4a) Of the above claim(s) *5,9-20,25,27,29 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,21-24,26,28 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-4,6-8,21-24,26,28,30 are presented for examination. Claims 5,9-20,25,27,29,31 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2,3, 8, 28,30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurosawa et al. (5,881,264) .

3. As to claims 1, 2, 8, Kurosawa disclosed a system with a main memory with a scoreboard comprising at least :

a) associating an instruction (fig.3, col.6, lines 23-36, see also fig.2 for background structure of the scoreboard [11]) with an index [3758ec] into the scoreboard, the index identifying the instruction [READ] ;

b) associating the instruction with a scoreboard entry (No.2) corresponding to the index (see the READ instruction in fig.3);

c) receiving an indication (synchronization) that a terminal event associated with the instruction has occurred (see the memory access instruction completion in col.9, lines

1-7) , the indication including identifying [see the index of READ instruction3758ec] and invalidating (see the Invalid bit entry in fig.3) based on the received scoreboard (see the invalid bit (I) in col.8, lines 4-12, lines 49-53).

4. As to claim 3, since no specific format of "a load instruction" has been reflected into the claim, the READ instruction is interpreted as a load instruction because a load means reading from memory, a store means writing into memory . As to the long latency instruction, a read instruction is a long latency instruction because it takes longer time to read from a memory than from a register.

5. As to claim 28, Kurosawa also included :

a) a scoreboard unit that included plurality of entries [entries] configurable to be indexed with scoreboard indices, the scoreboard unit configurable to indicate in each entry validity information [I] [V] for each instruction (see invalid and valid bits in corresponding entries in scoreboard in fig.5);

b) an execution unit configurable to maintain scoreboard indices for respective instructions and to scoreboard indices for use for locating and invalidating the respective entries (see the entry numbers in fig.3, see execution in co1.6, lines 33-52).

6. As to claim 30, Kurosawa also unlocked the entry (order =0) , and stalled the instruction dependent on the operands in the entries (see the order flag in the

scoreboard fig.43), locked the entry (order flag = 1) if indicated valid (v) , and unlocked (order flag= 0) if invalid (1)).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4,6,7, 21,22,23,24,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosawa 5,881 ,264 in view of Ramagopal et al. (6,473,832)

8. As to claims 4, 6,7, limitations of the parent clams have been discussed in paragraph #1 , therefore, it will not repeated herein. Kurosawa did not specifically show the load data has been received nor the forwarding (or receiving) the index value and the instruction to a load store processing unit as claimed. However, Ramagopal disclosed an indication of load data has been received (col.12, lines 16-63) and a load/store unit (e.g. see fig.l (26J). It would have been obvious to one of ordinary skill in the art to use Ramagopal in Kurosawa for including the indication of load data and forwarding (or receiving) the index value and the instruction to the load/store unit as claimed because the use of Ramagopal could provide Kurosawa the capability of the control circuit to adapt to particular access conditions of a given load or store instruction, thereby reducing the processing overheads of the control processor of Kurosawa, and it could be readily done by configuring the read/write pod of load/store unit of Ramagopal into Kurosawa with modified control parameters, such as the pod

width and data type, so that the load store unit of Ramagopal could be recognized by Kurosawa in order to achieve the enhanced system, and for the above reasons, provided a motivation.

9. As to claim 21 , Kurosawa also including locate an entry in a scoreboard for a n instruction with index returned from execution (see co1.6, lines 33-52), and invalidating the located entry (see the set and reset of the flags in scoreboard entry in col.6, lines 47-62, see also the invalidate bit I in the scoreboard entry in fig.3).

10. Kurosawa did not specifically show the load/store unit as claimed. However, Ramagopal disclosed a load/store unit (see fig.l (26)). It would have been obvious to one of ordinary skill in the art to use Ramagopal in Kurosawa for including the load/store unit as claimed, and the reasons of obviousness have been given in the paragraph above, therefore, it will not be repeated herein.

11. As to claim 22, Kurosawa also installed instruction into the scoreboard entries (see the instructions in the scoreboard entries in fig.3).

12. As to claim 23, Kurosawa also taught a terminal event [completion] associated with the instruction has occurred (see the memory access instruction completion in col.9, lines 1-7) ,

13. As to claim 24, as to the long latency instruction, a read instruction is a long latency instruction because it takes longer time to read from a memory than from a register.

14. Kurosawa et al. (5,881,264) and Ramagopal et al. (6,473,832) were already cited to applicant in the record previously, therefore copies are not provided herein.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)Gottlieb et al. (6,016,542) is cited for the teaching of the scoreboard entries with the index and validation information (see fig.3, col.5, lines 11-50) .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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